Detailed Action

1. This action is responsive to communication filed on: 17 June 2011 and Applicant Interview on 24 June2011, with acknowledgement of priority date of 23 August 2002, based on provisional application filing of 60/405,537.

2. Claims 30-54, are pending; claims 30, 41, and 47 are independent claims.

Response to Arguments

3. After review of Applicant's response and in consideration of the Applicant Interview: The 112 first rejection is removed, however the 112 second rejection is maintained, please see the below rejection for more clarification.

The claim objection is maintained as explained during the interview this an objection; if the application was ever considered allowable the briefest allowable claim would need to be identified for publication.

In addition a 101 rejection has been placed on claims 48-52 and 54 because of clarification provided by the 101 panel that when the preamble states "A non-transitory computer readable medium" the dependent claims also need to contain the term "non-transitory".

For the claim rejection address typographical errors "eachother" in the claims an amendment is needed.

After review and consideration of the application history the outstanding prior art rejection has been changed to best suit the Examiner's interpretation of the claim limitations, that the 'content processing' unit is a set-top box and the 'interchip content pathways' are internal to the set-top box.

4. Applicant's arguments filed 17 June 2011 as well as 8 February 2010 have been fully considered however they are moot due to new grounds of rejection or are not persuasive where noted below.

I) In response to Applicant's argument beginning on page 5, of Applicant's 17 June 2011 response, "Obviousness can only be established ... Neither Coli nor Candelore '489, taken alone or in combination disclose or suggest the claimed invention ... "relate to interchip data protection".

The Examiner disagrees both Coli and Candelore protect content inside a chip. In addition Candelore protects content being transferred between chips, see col. 6, lines 27-44. The content that is transferred between chips is encrypted therefore it is protected.

II) In response to Applicant's argument beginning on page 5, of Applicant's 17 June 2011 response, "Mauro also does not protect interchip communications. Maruo evens explicitly teaches away from the invention by teaching to eliminate the interchip communications. Specifically, Maruo integrates the security chip and the decoding chip in order to eliminate communications between these chip. See Fig. 3 an abs".

The Examiner disagrees Maruo teaches protecting interchip communication, note the abstract states "There are no points between the first function block (i.e. first chip package) and the decryption engine integral to the second functional block (i.e. second chip package) at which a descrambled and decrypted signal can be intercepted" this is 'protecting interchip communication'.

Claim Objections

5. Claims 30-54 are objected to because of the following informalities: According to 37 CFR 1.75 Claims (g) and MPEP 608.01(e) [R-3] the independent claims should be presented in order, with the least restrictive claim to be presented as claim number 1. In the interest of compact prosecution the Examiner finds Applications with the claims presented in the proper order make it easier to determine allowable subject matter. Independent claims 41 and 47 are less restrictive than claim 30. Appropriate correction is required.

6. Claims 30-54 are objected to because of the following informalities: the amended claim end with "eachother" with no space between the words. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 30-54 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims contain the phrase "wherein the first chip package, the second chip package and the interchip content pathway are contained in a single device without an interface between eachother". This limitation conflicts with the previous claim limitation "an interchip content pathway connecting the first chip package and the second chip package within said content processing unit". As best understood the underlined claim limitation means something to the effect "wherein content traveling between the first chip package, the second chip package, and on the interchip content pathway is protected".

Claim Rejections - 35 USC § 101

9. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. Claims 48-52 and 54, are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims are directed to "a computer readable medium", these claims are rejected under 101 because computer-readable medium can be interpreted as a signal, which is non-statutory subject matter.

In order to overcome the 101 rejection, the Examiner recommends that the language of the claim be modified to include "non-transitory".

11. To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. 112 and 101 above are further rejected as set forth below in anticipation of applicant amending these claims to overcome the 112 and 101 rejections.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. **Claims 30, 32-54,** are rejected under 35 U.S.C. 103(a) as being unpatentable over Candelore U.S. Patent 6,697,489 (hereinafter '489) in view of Craft et al. US Patent Application Publication 20020150243 (hereinafter '243) in further view of Maruo et al. U.S. Patent 7,146,007 (hereinafter '007).

As to independent claim 30, "A content processing unit for protecting interchip content pathways transporting content, the content processing unit comprising: a first chip package which receives content, wherein the first chip package comprises: a first body, an encryption engine, and a first key storage register capable of storing an interchip key, wherein:" is taught in '489 col. 6, lines 16-58;

"the interchip key is used by the encryption engine to produce ciphertext content from the received content" is shown in '489 col. 5, lines 51-62 the encryption engines with interchip keys are used to produce ciphertext context in;

"the first key storage register is non-readable from outside the first body, and" is disclosed in '489 col. 6, lines 16-58;

"a second chip package, wherein the second chip package comprises: a second body, a decryption engine, and a second key storage register capable of storing the interchip key, wherein: the interchip key is used by the decryption engine to produce plaintext content from the ciphertext content received from the first chip package, and the second key storage register is non-readable from outside the second body, the second key storage register being writeable while being non-readable; and an interchip content pathway connecting the first chip package and the second chip package within said content processing unit, the interchip content pathway carrying the ciphertext content from the

first chip package to the second chip package; and an output configured to provide the plaintext content to a user device capable of providing content to a user" is taught in '489 col. 6, lines 27-58 a smartcard (i.e. second chip package) is used with a conditional access module to decrypt content received and how the secure content is protected by using the secure keys;

the following is not explicitly taught in '489: **"the first key storage register cannot be overwritten after a programmability period, the programmability period being a period in which the interchip key is loaded in the first key storage"** however '243 teaches in paragraph 0042 "Each client CPU chip has a cryptographic unit that has been manufactured to contain programmable memory storage. Prior to releasing a client CPU chip, the manufacturer permanently embeds or fixes the assigned client serial number, the assigned client private key, and the server public key into the CPU chip. As shown in FIG. 2, client CPU chip 212 contains cryptographic unit 214, which includes client serial number 216, client private key 218, and server public key 220. A variety of well-known methods are available for embedding binary data within semiconductor chips, such as blowing semiconductor fuses as is used in DRAM manufacturing".

It would have been obvious to one of ordinary skill in the art at the time of the invention of secure receiving and decrypting digital content taught in '489 to include a means to program permanent keys into storage. One of ordinary skill in the art would have been motivated to perform such a modification to maintain control of distributed copyrighted content see '243 (page 2,

paragraphs 13-14).

the following is not explicitly taught in '243 and '489: **"wherein the first chip package, the second chip package and the interchip content pathway are contained in a single device without an interface between eachother"** however '007 teaches a secure path with a first functional block and s second functional block where the signal cannot be intercepted in the Abstract as well as col. 3, lines 41-59.

It would have been obvious to one of ordinary skill in the art at the time of the invention of secure receiving and decrypting digital content taught in '243 and '489 to protect content between chip packages. One of ordinary skill in the art would have been motivated to perform such a modification because the prior art system provide opportunities for the content to be pirated see '007 (col. 2, lines 5-67).

As to dependent claim 32, "wherein the programmability period ends after writing to the first key storage register" is shown in '243 paragraph 42.

As to dependent claim 34, wherein: the first chip package further stores a key encryption key, the interchip key is encrypted with the key encryption key, and the second chip package obtains the interchip key by decrypting the interchip key using the key encryption key" is taught in '489 col. 6, lines 27-36, note the second chip package in this embodiment is interpreted to be the unique descrambler IC key stored in register 450, and the first chip package is the smartcard.

As to dependent claim 35, "further comprising a plurality of content processing chip packages, each content processing chip package of the plurality of content processing chip packages having a unique key as the key encryption key, the unique key of each content processing chip package being distinct from the unique key of each other content

processing chip package" is shown in '489 col. 7, lines 11-19, note because it is a manufacturing process there are a plurality of smart cards that are paired with a respective plurality of to a specific host Descrambler IC.

As to dependent claim 36, "wherein each of the plurality of content processing chip packages receives a ciphertext message and obtains a unique interchip key by using the unique key to decrypt the message, the unique interchip key of each content processing chip package being distinct from the unique interchip key of each other content processing chip package" is taught in '489 col. 7, lines 15-20.

As to dependent claim 37, "wherein the second key storage register is overwritable" is shown in '489 col. 7, lines 15-20.

As to dependent claim 38, "wherein: the second chip package further comprises a second encryption engine, and the second encryption engine uses the interchip key or another key that is a function of the interchip key" is taught in '489 col. 7, line 59 through col. 8, line 19.

As to dependent claim 39, "further comprising a third chip package comprising a second interchip key that can decrypt second ciphertext content produced with the second encryption engine at the second chip package" is shown in '489 col. 7, lines 59-65.

As to independent claim 40, "wherein the third chip package is connected to the second chip package by a second interchip content pathway, the second interchip content pathway carrying the second ciphertext content from the first chip package to the second chip package" is taught in '489 col. 7, lines 15-20, i.e. third equivalent to replaced.

As to independent claim 41, "A method for protecting interchip content pathways transporting content within a content processing unit, the method comprising steps of: encrypting digital content at a first chip package with an interchip key to produce ciphertext content" is taught in '489 col. 6, lines 16-58;

"wherein the interchip key in the first key storage register is non-readable from outside the first chip package" is taught in ''489 col. 6, lines 16-58;

"coupling the ciphertext content from the first chip package to an interchip content pathway" is taught in '489 col. 5, line 57 through col. 6, line 4 coupling chip packages in a content pathway, i.e. interface;

"coupling the ciphertext content from the interchip content pathway to a second chip package; and decrypting the ciphertext content with the interchip key to reformulate the digital content" is shown in '489 col. 6, lines 27-58a smartcard (i.e. second chip package) is used with a conditional access module to decrypt content received and how the secure content is protected by using the secure keys;

"wherein the interchip key in the second key storage register is non-readable from outside the second chip package, the second key storage register being writable while being non-readable, and" is taught in '489 col. 7, lines 1-10, the use of a smartcard to process encrypted content, key storage register of smartcard are non-readable in addition as shown in '489 a key is programmed into the smartcard;
the following is not explicitly taught in '489:

"the interchip key being previously loaded into a first key storage register in a first chip package" and **"wherein the interchip key was previously loaded into a second key**

storage register in the second chip package" however '243 teaches in paragraph 0042 "Each client CPU chip has a cryptographic unit that has been manufactured to contain programmable memory storage. Prior to releasing a client CPU chip, the manufacturer permanently embeds or fixes the assigned client serial number, the assigned client private key, and the server public key into the CPU chip. As shown in FIG. 2, client CPU chip 212 contains cryptographic unit 214, which includes client serial number 216, client private key 218, and server public key 220. A variety of well-known methods are available for embedding binary data within semiconductor chips, such as blowing semiconductor fuses as is used in DRAM manufacturing".

It would have been obvious to one of ordinary skill in the art at the time of the invention secure receiving and decrypting digital content taught in '489 to include a means to program permanent keys into storage. One of ordinary skill in the art would have been motivated to perform such a modification to maintain control of distributed copyrighted content see '243 (page 2,
paragraphs 13-14).
the following is not explicitly taught in '243 and '489**:**

"wherein the first chip package, the second chip package and the interchip content pathway are contained in a single device without an interface between eachother" however '007 teaches a secure path with a first functional block and s second functional block where the signal cannot be intercepted in the Abstract as well as col. 3, lines 41-59.

It would have been obvious to one of ordinary skill in the art at the time of the invention of secure receiving and decrypting digital content taught in '243 and '489 to protect content between chip packages. One of ordinary skill in the art would have been motivated to perform

such a modification because the prior art system provide opportunities for the content to be pirated see '007 (col. 2, lines 5-67).

As to dependent claim 42, "further comprising steps of: loading a key encryption key into the first chip package; and decrypting the interchip key with the key encryption key, whereby the interchip key is protected with the key encryption key outside the first chip package" is taught in '243 paragraph 42.

As to dependent claim 43, "further comprising a step of overwriting the interchip key in the second key storage register from outside the second chip package" is shown in '489 col. 7, lines 15-19, overwriting same as replaced or changing keys to new host.

As to dependent claim 44, "further comprising steps of: encrypting the digital content in the second chip package to produce second ciphertext content using a second interchip key, coupling the second ciphertext content to a second content pathway" is disclosed in '489 col. 5, line 63 through col. 6, line 5.

As to dependent claim 45, "further comprising: providing a unique interchip key to each of a plurality of content processing chip packages, the unique interchip key of each content processing chip package being distinct from the unique key of each other content processing chip package and protecting a respective content pathway to each content chip processing package" is shown in '489 col. 7, lines 11-19, note because it is a manufacturing process there are a plurality of smart cards that are paired with a respective plurality of to a specific host Descrambler IC.

As to dependent claim 46, "wherein the step of providing a unique interchip key includes providing a message to each of the plurality of content processing chip packages,

and each content processing chip package decrypts the message to obtain a unique interchip key" is disclosed in '489 col. 7, lines 15-19.

As to independent claim 47, this claim is directed a computer readable medium containing instructions for a computer to perform a method of independent claim 41; therefore it is rejected along similar rationale.

As to dependent claims 48-52, these claims contain substantially similar subject matter as claims 42-47; therefore they are rejected along similar rationale.

14. **Claims 31, 33, 53, and 54,** are rejected under 35 U.S.C. 103(a) as being unpatentable over Candelore U.S. Patent 6,697,489 (hereinafter '489) in view of Craft et al. US Patent Application Publication 20020150243 (hereinafter '243) in further view of Maruo et al. U.S. Patent 7,146,007 (hereinafter '007) in further view of Coli U.S. Patent No. 5,452,355 (hereinafter '355).

As to dependent claim 31, the following is not explicitly taught in '489, '243, and '007: **"further the first chip package includes a fusable link, wherein the first key storage register cannot be overwritten after the fusable link is activated"** however '355 teaches the use of a fusable line in col. 4, lines 8-52.

It would have been obvious to one of ordinary skill in the art at the time of the invention of secure receiving and decrypting digital content taught in '243, '007, and '489 to include a fusable link. One of ordinary skill in the art would have been motivated to perform such a modification because the high level of pirating of circuits on the markplace to develop more stringent levels of security see '355 (col. 1, lines 38 et seq.).

As to dependent claim 33, "wherein at least one of the first and second chip packages comprises a plurality of semiconductor substrates" is disclosed in '355 col. 1, lines 31-37 and col. 4, lines 40-42.

As to dependent claim 53, "wherein the interchip key in the first key storage register is rendered into a non-readable from outside the first chip package by activating a feature of the first chip package that prevents overwriting the interchip key in the first key storage register from outside the first chip package, after a period in which the first key is loaded in the first key storage" is taught in '355 col. 4, lines 8-52.

As to dependent claim 54, this claim contains substantially similar subject matter as claim 53; therefore it is rejected along similar rationale.

Conclusion

15. It is noted, PATENTS ARE RELEVANT AS PRIOR ART FOR ALL THEY CONTAIN "The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned. They are part of the literature of the art, relevant for all they contain." In re Heck, 699 F.2d 1331, 1332-33, 216 USPQ 1038, 1039 (Fed. Cir. 1983) (quoting In re Lemelson, 397 F.2d 1006, 1009, 158 USPQ 275, 277 (CCPA 1968)). A reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill the art, including nonpreferred embodiments (see MPEP 2123).

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ellen C Tran whose telephone number is (571) 272-3842. The examiner can normally be reached from 7:30 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivek Srivastava can be reached at (571) 272-7304. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

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/ELLEN TRAN/
Primary Examiner, Art Unit 2433
29 August 2011